Amendments to the Specification:

On page 1, please amended the title to read --PHASE INTERPOLATOR AND RECEIVER FOR ADJUSTING CLOCK PHASES INTO DATA PHASES--.

Please replace paragraph 0004 with the following amended paragraph:

[0004] FIG. 11 is a block diagram showing a high-speed input/output (I/O) device. A transmitter 4 converts input parallel data 1 into serial data 2. In this specification, the serial data is differential pair signals from CML (current mode logic). The converted serial data 2 is transmitted to a receiver 5. The receiver 5 receives the serial data 2 and converts it into parallel data 3. The serialization of parallel data into serial data and the deserialization of serial data into parallel data are carried out in synchronization with clock signals. The serial data 2 from the transmitter 4 is asynchronous with the clock signals of the receiver 4. To correctly read the serial data 2 in the receiver 5, the serial data 2 must be synchronized with the clock signals. To achieve this, the phases of the clock signals must be ~~adjusted to~~ synchronized with those of the serial data 2. To provide a function of adjusting the phases of clock signals to those of serial data, a phase interpolator (abbreviated as PI) and a data read circuit are employed.

Please replace paragraph 0030 with the following amended paragraph:

[0030] FIG. 1 is a block diagram showing a receiver according to an embodiment of the present invention. The receiver includes a data read circuit 6 and a phase interpolator 7. The phase interpolator 7 receives four-phase (0, .pi./2, .pi., 3.pi./2) clock signals (Clock_In, CML) 8 and provides four-phase clock signals (Reclock_In) 9 whose phases are synchronous with those of serial data 2'. The serial data 2', is sent from a transmitter (not shown) to the data read circuit 6. The data read circuit 6 reads the serial data 2' based on the clock signals 9, provides the phase interpolator 7 with a phase information signal (UP/DN) 10 containing information about the phases of the clock signals and serial data 2\ and outputs data 11, which is synchronous with

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clock signals in the receiver, and clock signals 9', which have phases ~~adjusted to~~ <u>synchronized</u> <u>with</u> those of the data 11, to subsequent circuits for further processing.

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